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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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09/772,883

01/31/2001

Seiji Fujiwara

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7590

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Beveridge, DeGrandi,  
Weilacher & Young, L.L.P.  
Suite 800  
1850 M Street, N.W.  
Washington, DC 20036

EXAMINER

SHINGLETON, MICHAEL B

ART UNIT

PAPER NUMBER

2817

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 09/772,883	Applicant(s) FUJIWARA ET AL.	
	Examiner Michael B. Shingleton	Art Unit 2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- the RCE request
- 1) ☒ Responsive to communication(s) filed on 5/17/04
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 ~~is~~ are pending in the application.
- 4a) Of the above claim(s) 4, 5, 8 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15-19 ~~is~~ are allowed.
- 6) ☒ Claim(s) 1-3, 6, 9-12 ~~is~~ are rejected.
- 7) ☒ Claim(s) 7, 13 and 14 ~~is~~ are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>May 17, 2004</u> | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-3, 6 and 9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Katz et al. 5,038,113(Katz).

Figure 11 of Katz discloses a predistortion circuit having an input terminal 90 for inputting a predetermined signal, a non-linear device 88 directly or indirectly connected to the input terminal, a bias supply circuit (Note  $V_{BIAS}$ ) that applies a voltage to the non-linear device and a “specific” frequency suppressing means 1124 and 1125 connected to one side or both sides of the non-linear device 88 directly without another intervening device. The specific frequency suppressing means suppresses all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied bandwidth of an input signal inputted to the input terminal. Note that since elements 1124 and 1125 are inductors the DC/low frequency component will be suppressed, i.e. shorted to ground because an inductor is considered to be a short insofar as such a signal is concerned which is common engineering knowledge. The non-linear element clearly would present a much larger impedance at such frequencies. Element 92 is an output terminal that is connected to a power amplifier (See the paragraph bridging columns 4 and 5). Figure 11 of Katz clearly illustrates the nonlinear device as being provided between the connection point between the input terminal and the output terminal and the ground.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Katz et al. 5,038,113 (Katz) in view of Yun et al. 5,914,641 (Yun) and Fukuden 5,805,023 (Fukuden).

Figure 11 of Katz discloses a predistortion circuit having an input terminal 90 for inputting a predetermined signal, a non-linear device 88 directly or indirectly connected to the input terminal, a bias supply circuit (Note  $V_{BIAS}$ ) that applies a voltage to the non-linear device and a “specific” frequency suppressing means 1124 and 1125 connected to one side or both sides of the non-linear device 88 directly without another intervening device. The specific frequency suppressing means suppresses all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied bandwidth of an input signal inputted to the input terminal. Note that since elements 1124 and 1125 are inductors the DC/low frequency component will be suppressed, i.e. shorted to ground because an inductor is considered to be a short insofar as such a signal is concerned which is common engineering knowledge. The non-linear element clearly would present a much larger impedance at such frequencies. Element 92 is an output terminal that is connected to a power amplifier (See the paragraph bridging columns 4 and 5). Figure 11 of Katz clearly illustrates the nonlinear device as being provided between the connection point between the input terminal and the output terminal and the ground. Katz is silent on the exact form of the power amplifier.

Figure 12 of the Fukuden reference discloses the same amplifier circuit as claimed except that the bias networks are not shown. Note that elements like 21, 21', 22, 22' of Fukuden meet the claimed limitations to the frequency suppressing means like that shown as elements 1307 and 1309 in the disclosed invention. The amplifier structure of Fukuden is a conventional art recognized equivalent amplifier structure. Accordingly, it would have been obvious to one of ordinary skill in the art at the time of the invention to have added the amplifier of Fukuden for the amplifier of Katz because, as the Katz is silent on the exact structure of the amplifier one of ordinary skill in the art would have been motivated to use any art recognized equivalent amplifier circuit such as the conventional amplifier of Fukuden.

Yun discloses the conventional use of bias(supply) means VDD and VGG to supply the necessary biases to properly bias the transistor to the active region and accordingly to operate the transistor in the proper operation class.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the conventional bias supply means like that of Yun in Katz in combination with Fukuden above so as to properly bias the transistor to the active region and accordingly to operate the transistor in the proper operation class as taught by Yun.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katz et al. 5,038,113(Katz).

Figure 11 of Katz discloses a predistortion circuit having an input terminal 90 for inputting a predetermined signal, a non-linear device 88 directly or indirectly connected to the input terminal, a bias supply circuit (Note  $V_{BIAS}$ ) that applies a voltage to the non-linear device and a “specific” frequency suppressing means 1124 and 1125 connected to one side or both sides of the non-linear device 88 directly without another intervening device. The specific frequency suppressing means suppresses all or part of such frequencies that are from a frequency corresponding to DC to a frequency corresponding to an occupied bandwidth of an input signal inputted to the input terminal. Note that since elements 1124 and 1125 are inductors the DC/low frequency component will be suppressed, i.e. shorted to ground because an inductor is considered to be a short insofar as such a signal is concerned which is common engineering knowledge. The non-linear element clearly would present a much larger impedance at such frequencies. Element 92 is an output terminal that is connected to a power amplifier (See the paragraph bridging columns 4 and 5). Figure 11 of Katz clearly illustrates the nonlinear device as being provided between the connection point between the input terminal and the output terminal and the ground. The frequency suppressing means shown by Katz are only shown schematically as a single inductor. Katz is silent on the exact makeup of this inductor means.

Nevertheless, as one of ordinary skill in the art would have known, a plurality of lumped inductor components connected in series is the art recognized equivalent to a single inductor.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the individual inductor means 1124 and 1125 of Katz with a series combination of lumped inductor elements having the overall inductance of these elements because, as the Katz reference is silent on the exact makeup of the inductor arrangement in question one of ordinary skill in the art would have been motivated to use any art-recognized equivalent inductor arrangement such as the conventionally known series combination of lumped inductor elements.

Claims 7, 13, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 15-19 are allowed.

Art Unit: 2817

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571)272-1770. The examiner can normally be reached on Mon-Thurs from 8:30 to 4:30. The examiner can also be reached on alternate Fridays. The examiner normally has first Fridays of the bi-week off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS

June 16, 2004

*Michael B. Shingleton*  
MICHAEL B SHINGLETON  
PRIMARY EXAMINER  
GROUP ART UNIT 2817